REMARKS

Reconsideration of the present application is respectfully requested. Claims 11 and 23 have been amended. No claims have been canceled or added in this response. No new matter has been added.

Claim Rejections §102

Independent claims 1 and 19 stand rejected under 35 U.S.C. § 102(e) based on Blumenau et al. (hereinafter "Blum", U.S. Patent no. 6,421,711). Applicant respectfully traverses the rejections.

The present invention relates to a virtualization storage server implementing the virtualization functionality using separate storage processors connected by a switching fabric and controlled by a microcontroller.

Claim 1 recites:

> 1. A storage server in a storage area network connecting a plurality of host computers and a plurality of storage devices, said storage server comprising:
>
> a plurality of storage processors, wherein said plurality of storage processors receive a plurality of command packets and a plurality of data packets;
>
> a switching circuit connecting said plurality of storage processors; and
>
> a microengine, wherein said microengine is configured to execute processing comprising:
>
> configuring a path between a first storage processor and a second storage processor of said plurality of storage processors, via said switching circuit, in accordance with a command packet of said plurality of command packets; and
>
> **routing a data packet of said plurality of data packets over said path, prior to completely receiving said data packet, between said first storage processor and said second storage processor via said switching circuit.**

(Emphasis added)

In contrast, Blum does not teach or suggest the above emphasized limitations in claim 1, namely, routing a data packet of said plurality of data packets over said path, prior to completely

receiving said data packet, between said first storage processor and said second storage processor via said switching circuit. The Examiner cites Blum's column 10, lines 10-16 and 52-60, column 39, lines 34-55, column 40, lines 21-40 and column 41, lines 35-65, alleging these sections teach or suggest the above emphasized limitation. However, column 10, lines 10-16 discuss the concept of "private loop", "public loop", "fabric" and "switch". Column 10, lines 52-60 discuss Fiber Channel network, S_ID, etc. Column 39, lines 34-55 discuss a frame structure and reducing network traffic by eliminating some of the frames. Column 40, lines 21-40 discuss encryption. Column 41, lines 35-65 discuss an architecture of connecting host computers with multiple storage controllers. None of the above cited sections teaches or suggest routing a data packet of said plurality of data packets over said path, prior to completely receiving said data packet, between said first storage processor and said second storage processor via said switching circuit. Neither does the rest of Blum teach or suggest the limitation. Thus, at least for the above reasons, claim 1 and all claims which depend on it are patentable over Blum.

Independent claim 19 recites a limitation similar to that discussed above for claim 1. For similar reasons, claim 19 and all claims depend on it are patentable over Blum.

For the foregoing reasons, the present application is believed to be in condition for allowance, and such action is earnestly requested.

If any additional fee is required, please charge Deposit Account No. 02-2666.

Respectfully submitted,
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